REMARKS

Claims 37, 39 and 59 are amended. Claim 60 is canceled. Claims 24-31, 36, 37, 39-41 and 45-59 are in the application for consideration.

Independent claim 36 stands rejected as being obvious over a combination of '331 Hsu et al. in view of '240 to Lee. Applicant disagrees and requests reconsideration.

In pertinent part, independent claim 36 recites in one anisotropic etching step of the insulative sidewall forming layer, forming an insulative sidewall spacer on only the drain side and not on the source side. The applied Lee patent clearly only teaches forming insulative sidewall spacers simultaneously on both of the source side and the drain side. With respect to Hsu et al. spacer forming layer 252, Fig. 11a clearly only shows forming an insulative sidewall spacer on only the source side, and not on the drain side. Accordingly, Hsu et al. teach the opposite of that which Applicant recites in independent claim 36. The apparent Examiner rationale as to why Applicant's claim 36 would apparently be obvious over Hsu et al. is "that since a FET based device is symmetric the source and drain are interchangeable". However, this assertion is in error with respect to FLASH memory cells. FLASH memory cells are not conventional field effect transistors, and clearly their source and drains are not simply interchangeable. Specifically, the sources of FLASH memory cells in the context of Applicant's claims at least along a line of floating gates are everywhere electrically interconnected. However, the drains are not electrically interconnected. Further, source regions and drain regions of

FLASH memory cells typically have different and separately optimized implant doses. This is even apparent from the Examiner's applied Hsu et al. reference wherein in Fig. 14a, source regions 239 have different profiles and different dopant concentration than the drains (not designated by Hsu et al. with numerals) on the opposite side of the line of floating gates. Accordingly, the Examiner's assertion that sources and drains are interchangeable is fundamentally not true with respect to FLASH memory cells. Hsu et al. only teach initially forming an insulative sidewall spacer on only the source side and not the drain side, which is the opposite of that which Applicant claims. It simply would not be obvious to substitute one for the other, or reverse the order, and there is absolutely no suggestion or disclosure within Hsu et al. or any other reference of record referring to FLASH memory cells of forming an insulative sidewall spacer on only the drain side and not on the source side in one anisotropic etching step of an insulative sidewall forming layer in the manner in which Applicant claims. Accordingly, the rejection of Applicant's claim 36 over the cited art should be withdrawn, claim 36 should be formally allowed, and action to that end is requested.

Independent claim 37 has been amended to recite that the line of floating gates is formed over channel active area of the semiconductor substrate. The forming of the line of floating gates is further cited to comprise providing a gate dielectric layer intermediate floating gate material and the channel active area. Formation of the line of floating gates is further recited to comprise initially etching through the gate dielectric layer

on both of the source side and the drain side. The Examiner will note in each of Lee and Hsu et al., the respective indicated line of floating gates are formed by etching to stop on the gate dielectric layer, and therefore etching is not conducted through the gate dielectric layer in the manner which Applicant recites in claim 37. As neither reference discloses this facet of Applicant's amended claim 37, the combined references clearly do not do so.

Further, independent claim 37 is amended to recite the first insulative sidewall spacer and the second insulative sidewall spacers have innermost surfaces which are received on (meaning in contact with) semiconductive material of the semiconductor substrate. Support for the same is inherent from Applicant's application as-filed, for example, as shown in Fig. 9. Clearly neither Lee nor Hsu et al. disclose such a method. Rather, each teaching discloses that the innermost surfaces of the respective spacers are received on gate dielectric material, and therefore not on semiconductive material of their respective substrates.

Accordingly, amended claim 37 recites something which is neither shown nor suggested in either of the applied references. Accordingly, a combination of these references does not suggest that which Applicant recites in amended independent claim 37. Accordingly, the rejection of claim 37 should be withdrawn, claim 37 allowed, and action to that end is requested.

Dependent claim 39 is amended, and should be examined in this application and allowed as depending from an allowable base claim. Even if

the Examiner for some reason is inclined not to allow claim 36, examination of claim 39 on its merits is not seen to in any way add undue burden to the Examiner by its examination in light of the art. Regardless, dependent claim 39 should be allowed for its own recited features which are neither shown nor suggested in the art of record.

Claim 59 is amended, thereby obviating the Examiner's §112 rejection. Specifically, such claim depends from claim 36, and recites that the forming of the line of floating gates comprises initially etching through the gate dielectric layer on both of the source side and the drain side, with the insulative sidewall spacer on the drain side having an innermost surface which is received on semiconductive material of the semiconductor substrate. As argued above with respect to claim 37, neither the source side nor drain side spacers in either of Lee or Hsu et al. contacts semiconductive material of its semiconductor substrate, as blocking gate dielectric material is received there between. Accordingly, claim 59, as well as the other dependent claims that have been rejected, should be allowed as depending from allowable base claims as well as for their own recited features which are neither shown nor suggested in the cited art. Action to that end is requested.

The undersigned submitted a Supplemental Information Disclosure Statement with its RCE filing on September 30, 2002. However, the undersigned has not yet received an initialed copy of the PTO-1449 which was submitted with that Disclosure Statement. This was pointed out to the Examiner in Applicant's last-filed response, but the undersigned did not find

the requested initialed PTO-1449 form included with the most recent Office Action. Another duplicate copy of the PTO-1449 is included herewith. Perhaps, the PTO-1449 was initialed, but not mailed to Applicant. Regardless, it is respectfully requested that the Examiner send the undersigned a copy of the initialed PTO-1449.

This application is believed to be in immediate condition for allowance.

Respectfully submitted,

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By: _____
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